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PLUS Search Results for S/N 09752880, Searched September 30, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present. PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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09752880_CLS
Most Frequently Occurring Classifications of Patents Returned
From A Search of 09752880 on September 30, 2004

Original Classifications

2	324/158.1
2	365/63
2	710/100
2	710/107
2	710/307
2	710/310
2	713/501

Cross-Reference Classifications

3	365/52
2	324/73.1
2	711/141
2	712/1

Combined Classifications

3	324/73.1
3	365/52
3	710/310
2	324/158.1
2	326/37
2	326/47
2	365/63
2	710/100
2	710/105
2	710/107
2	710/307
2	711/141
2	712/1
2	713/401
2	713/501

09752880_CLSTITLES

Titles of Most Frequently Occurring Classifications of Patents Returned

From A Search of 09752880 on September 30, 2004

3 324/73.1 (1 OR, 2 XR)
Class 324 : ELECTRICITY: MEASURING AND TESTING
324/73.1 PLURAL, AUTOMATICALLY SEQUENTIAL TESTS

3 365/52 (0 OR, 3 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/52 HARDWARE FOR STORAGE ELEMENTS

3 710/310 (2 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/305 .Bus interface architecture
710/306 ..Bus bridge
710/310 ...Buffer or que control

2 324/158.1 (2 OR, 0 XR)
Class 324 : ELECTRICITY: MEASURING AND TESTING
324/158.1 MISCELLANEOUS

2 326/37 (1 OR, 1 XR)
Class 326 : ELECTRONIC DIGITAL LOGIC CIRCUITRY
326/37 MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.)

2 326/47 (1 OR, 1 XR)
Class 326 : ELECTRONIC DIGITAL LOGIC CIRCUITRY
326/37 MULTIFUNCTIONAL OR PROGRAMMABLE (E.G., UNIVERSAL, ETC.)
326/47 .Significant integrated structure, layout, or layout interconnections

2 365/63 (2 OR, 0 XR)
Class 365 : STATIC INFORMATION STORAGE AND RETRIEVAL
365/63 INTERCONNECTION ARRANGEMENTS

2 710/100 (2 OR, 0 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)

2 710/105 (1 OR, 1 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/105 .Protocol

2 710/107 (2 OR, 0 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/107 .Bus access regulation

2 710/307 (2 OR, 0 XR)
Class 710 : ELECTRICAL COMPUTERS AND DIGITAL DATA PROCESSING SYSTEMS: INPUT/OUTPUT
710/100 INTRASYSTEM CONNECTION (E.G., BUS AND BUS TRANSACTION PROCESSING)
710/305 .Bus interface architecture
710/306 ..Bus bridge
710/307 ...Variable or multiple bus width

2 711/141 (0 OR, 2 XR)
Class 711 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: MEMORY
711/100 STORAGE ACCESSING AND CONTROL
711/117 .Hierarchical memories
711/118 ..Caching
711/141 ...Coherency

2 712/1 (0 OR, 2 XR)
Class 712 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: PROCESSING ARCHITECTURES AND INSTRUCTION PROCESSING
712/1 PROCESSING ARCHITECTURE

2 713/401 (1 OR, 1 XR)
Class 713 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: SUPPORT
713/400 SYNCHRONIZATION OF CLOCK OR TIMING SIGNALS, DATA, OR PULSES
713/401 .Using delay

2 713/501 (2 OR, 0 XR)
Class 713 : ELECTRICAL COMPUTERS AND DIGITAL PROCESSING SYSTEMS: SUPPORT

09752880_CLSTITLES

713/500	CLOCK, PULSE, OR TIMING SIGNAL GENERATION OR ANALYSIS
713/501	.Multiple or variable intervals or frequencies